FPGA Implementation of Stereo Disparity with High Throughput for Mobility Applications

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System Motivation

- Develop a system to accelerate stereo camera ranging capable of high throughput processing
- Interface directly to stereo cameras
- Process imagery at or near camera frame rates
- Provide to host system full color camera imagery and output disparity measurements at high frame rates
- Fit in a small form factor FPGA board with low power consumption.

Why FPGA?

- FPGAs provide a flexible platform for providing a vehicle for flexible interconnects.
- Large number of logic blocks produces massive amounts of computational elements
- Large internal memories aids in keeping intermediate products on chip, reducing external memory bandwidth
- Stereo problem is “embarrassingly parallel.” Many computations are independent of each other
- Operations are invariant. Each pixel is operated on by the same set of processes.
- Design goal is heavily pipelined, 1 output per clock

Stereo Ranging

- Stereo ranging is the process of measuring distance by using two images taken simultaneously from slightly different points of view.
- Nine steps to stereo:

(1) Digitize the stereo image pair.

(2) Rectify the images

(3) Filter image using a bilateral subtraction filter to normalize the image pair and highlight features.

(4) Correlate, or measure image similarity by computing the Sum of Absolute Differences (SAD) for 7x7 windows over a fixed disparity search range.

(5) Estimate disparity by finding the SAD minimum independently for each pixel.

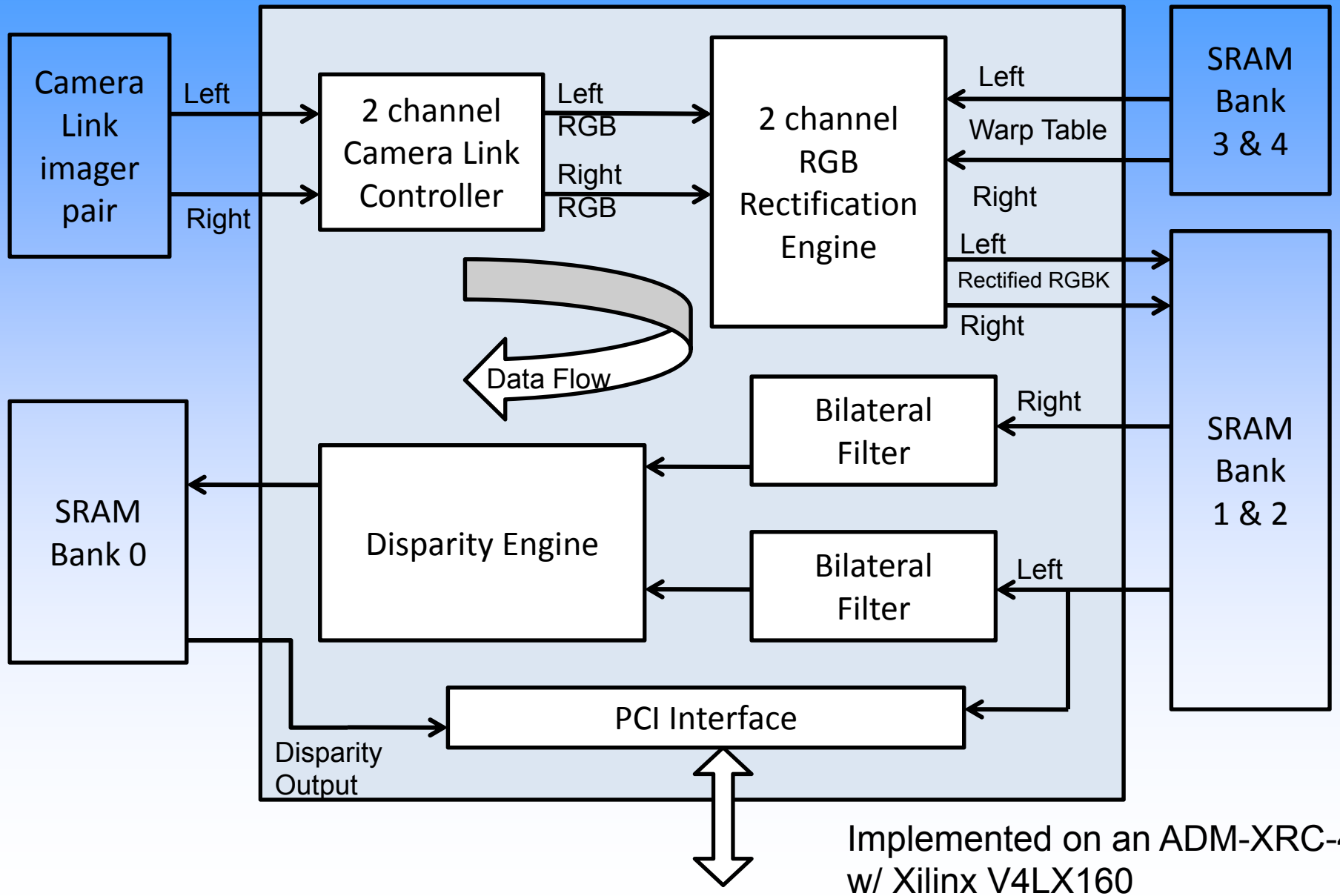
(6) Filter out bad matches by using the left-right-line-of-sight (LRLOS) consistency check.

(7) Estimate sub-pixel disparity by fitting parabolas to the three SAD values surrounding the SAD minimum and taking the disparity estimate to be the minimum of the parabola.

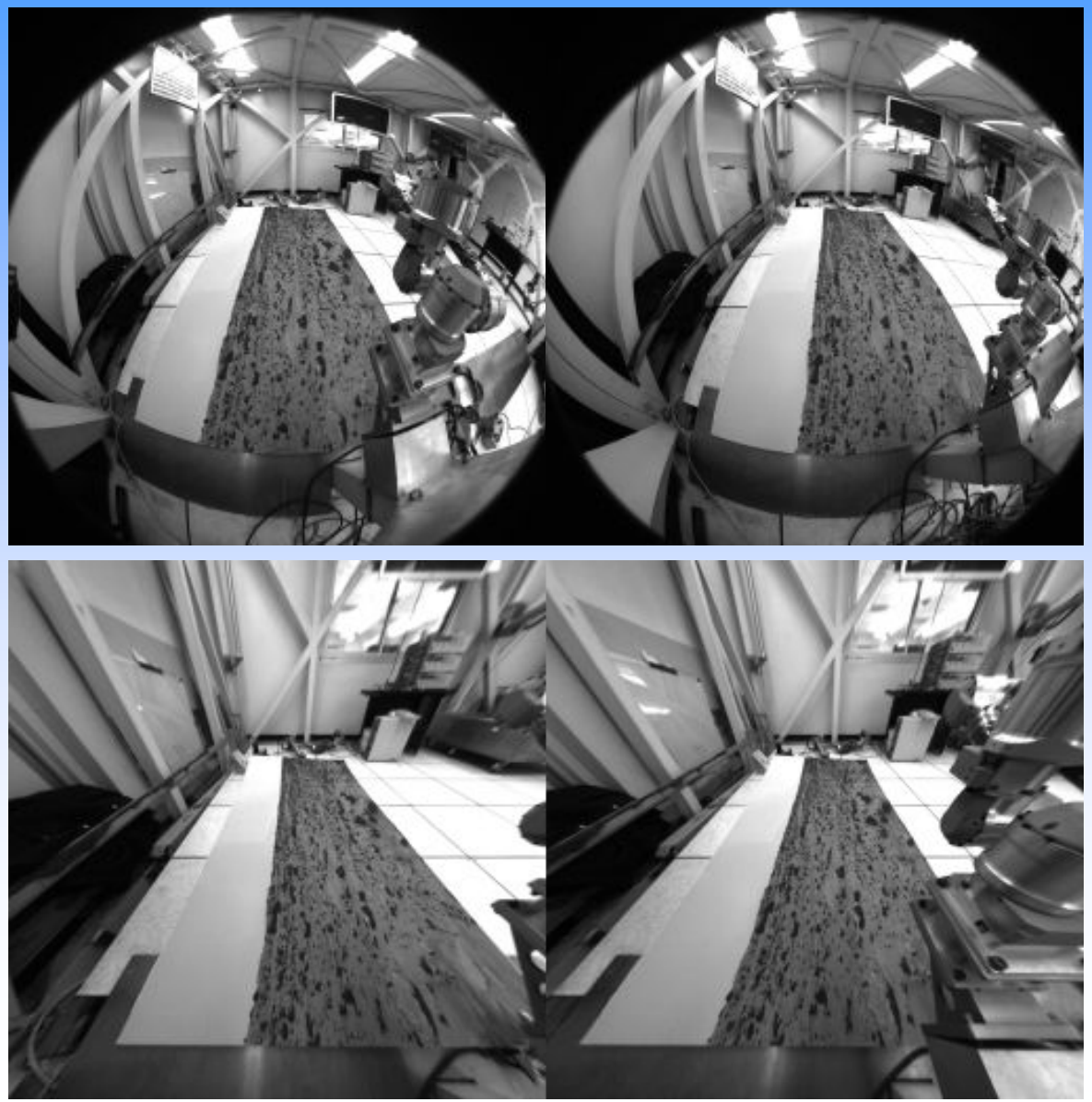
(8) Filter out small regions (likely bad matches) by applying a blob filter that uses a threshold on the disparity gradient as the connectivity criterion.

(9) Triangulate to produce the X-Y-Z coordinates at each pixel and transform to the vehicle co-ordinate frame.

System Overview

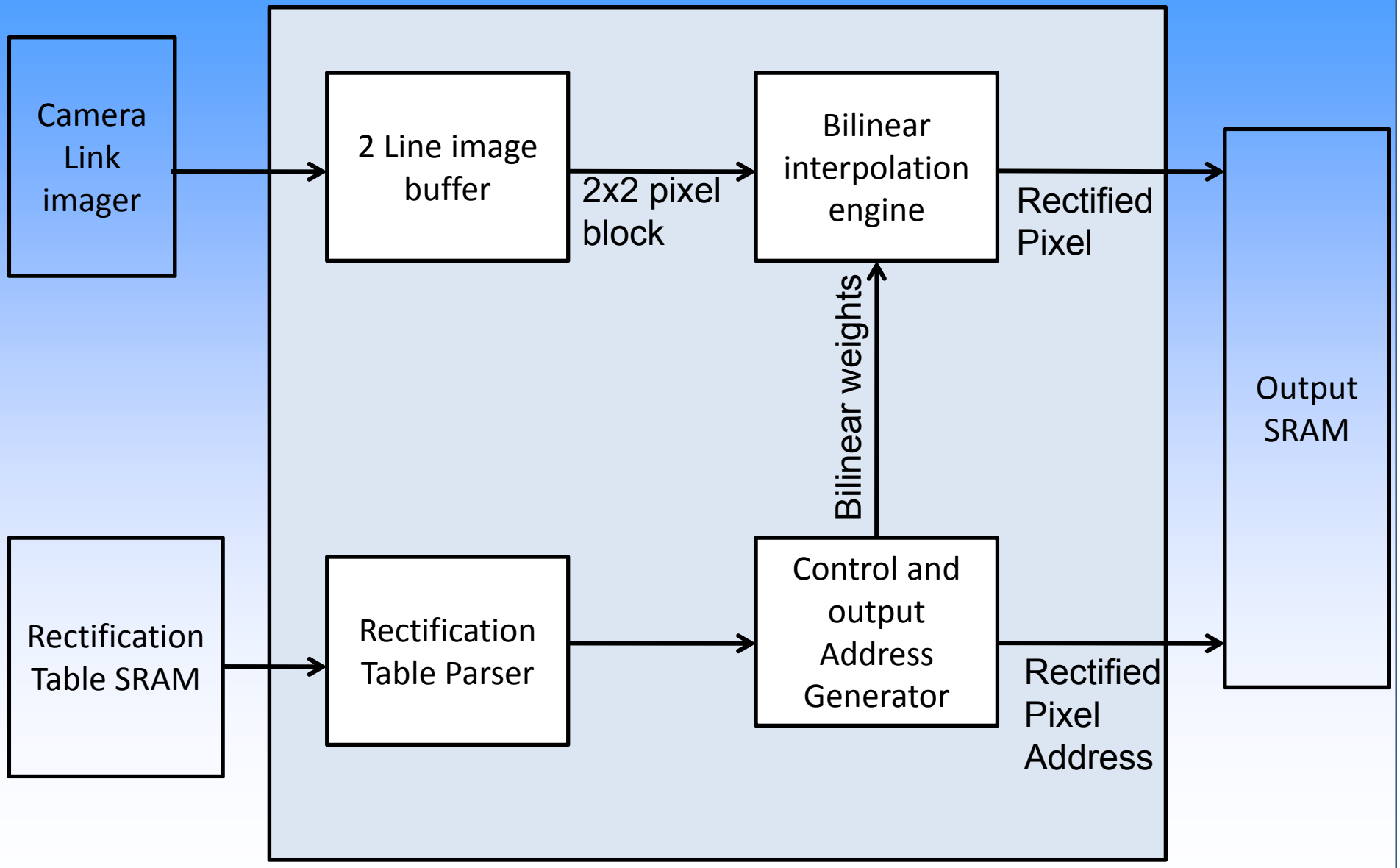


Rectification

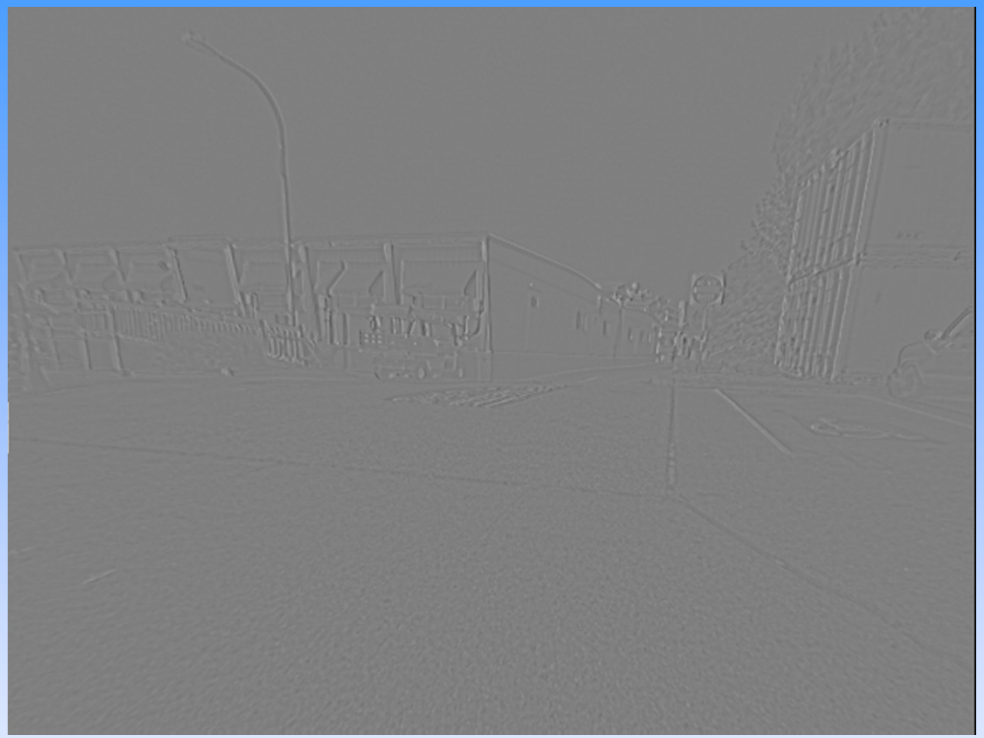


- **Removes camera system and lens distortion**
  - "De-warps" image to what an ideal pinhole camera would produce.
- **Corrects pointing errors**
  - Re-renders the image so that each has an axis that is parallel and colinear with the other image.
  - Simplifies stereo correlation reducing it to a line based search instead of area based.
- **Warp table pre-computed**
  - After calibration, a mathematical camera model is produced.
  - Practical applications pre-compute a warp table for each pixel from the camera model

Rectification Module



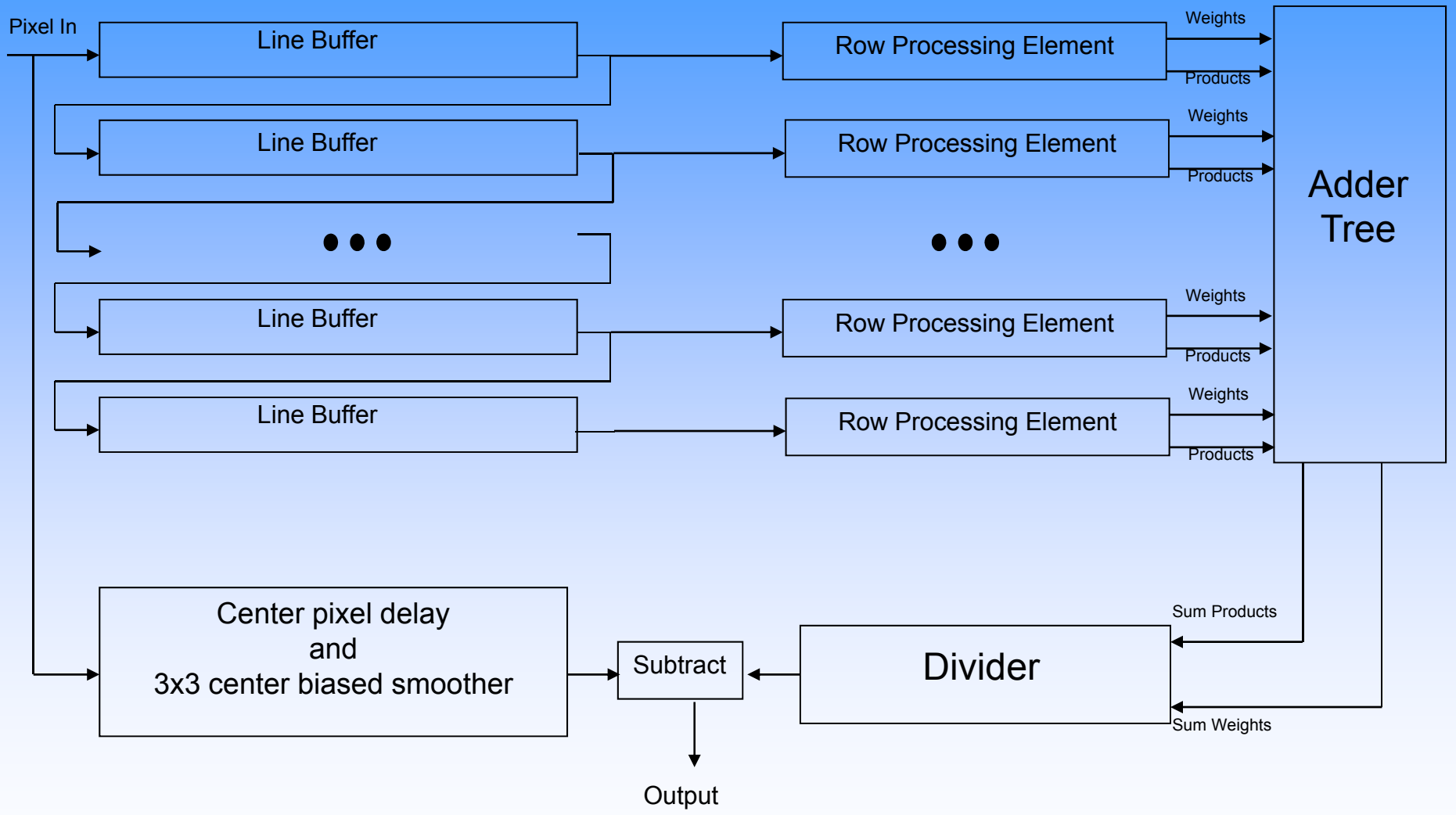
Filtering (Bilateral Subtraction)



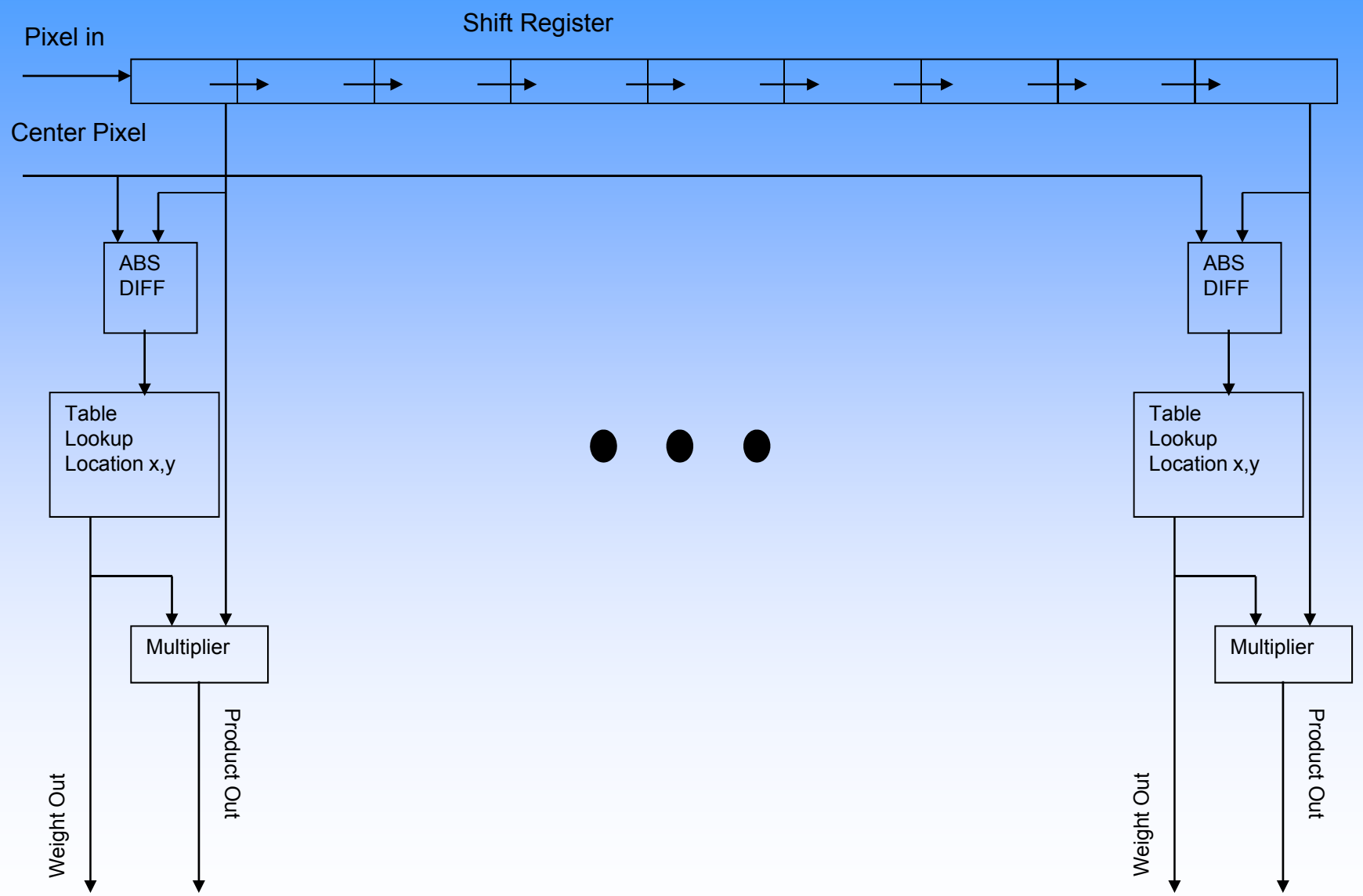
Filtering is performed to normalize the stereo pair to each other and to highlight edge information for better correlation matching.

A Bilateral Filter is a noise reducing, edge preserving filter. The filtered image is subtracted from the 3x3 smoothed original image.

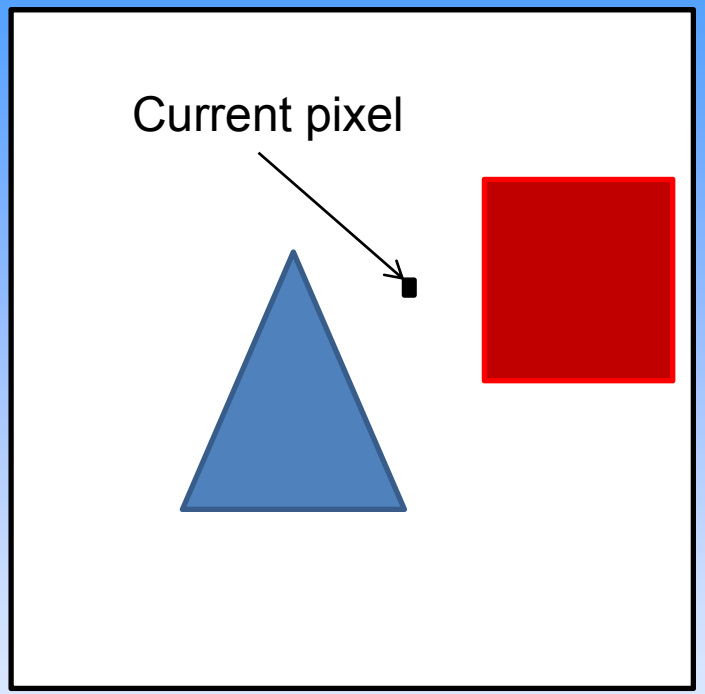
Bilateral Subtraction Filter



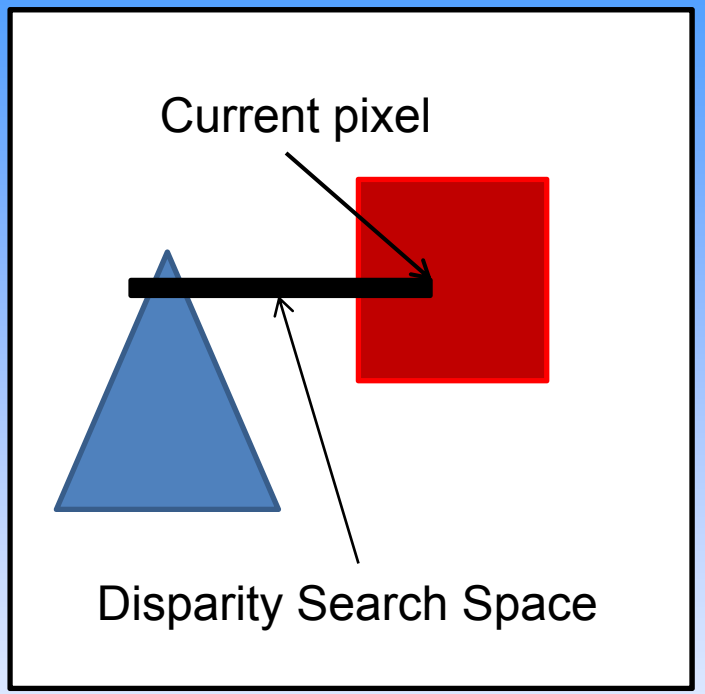
Filter (cont.)


Pixel in
Shift Register
Center Pixel
ABS DIFF
ABS DIFF
Table Lookup Location x,y
Table Lookup Location x,y
Multiplier
Multiplier
Weight Out
Product Out
Weight Out
Product Out

Correlation



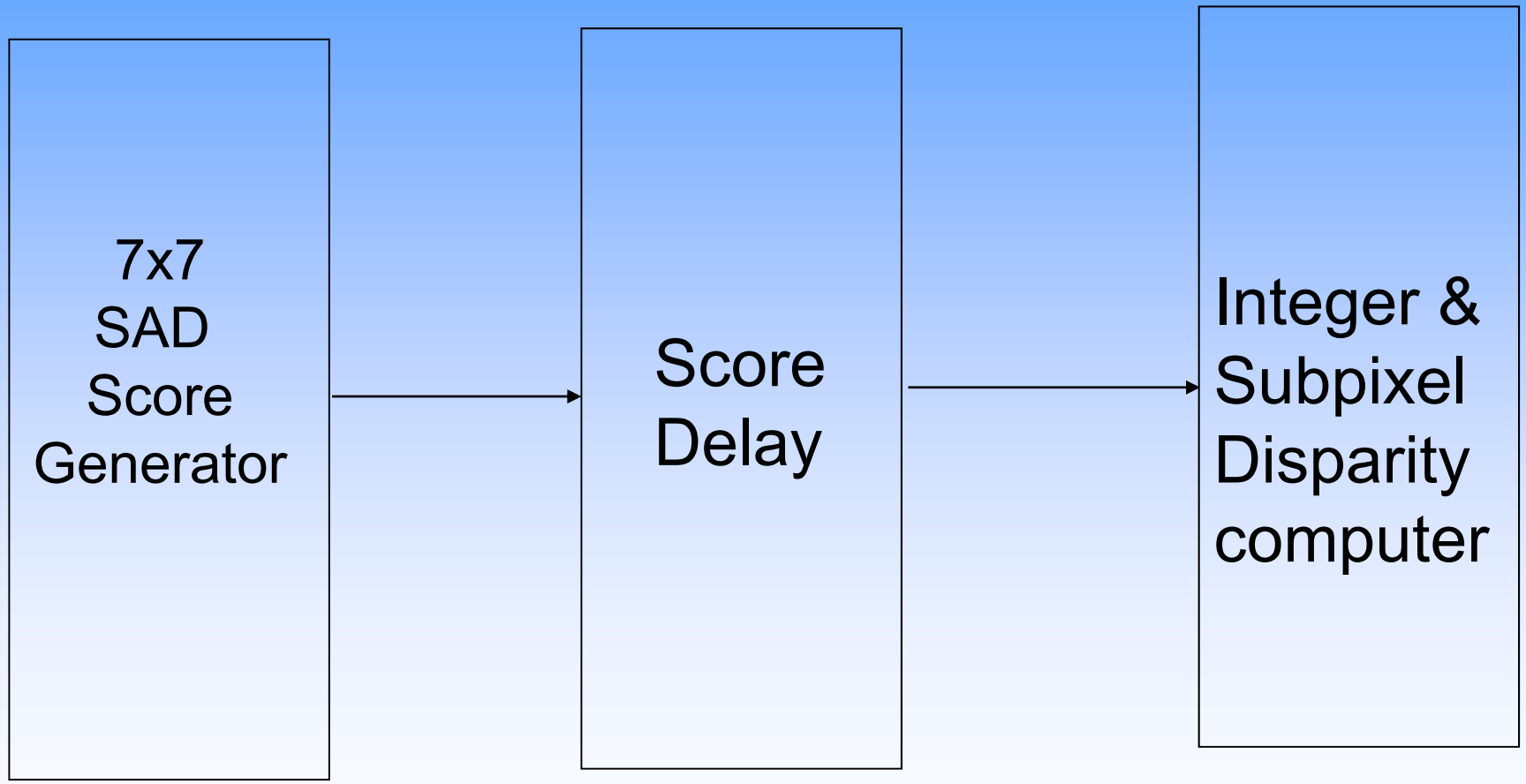
Left Image
(reference image)



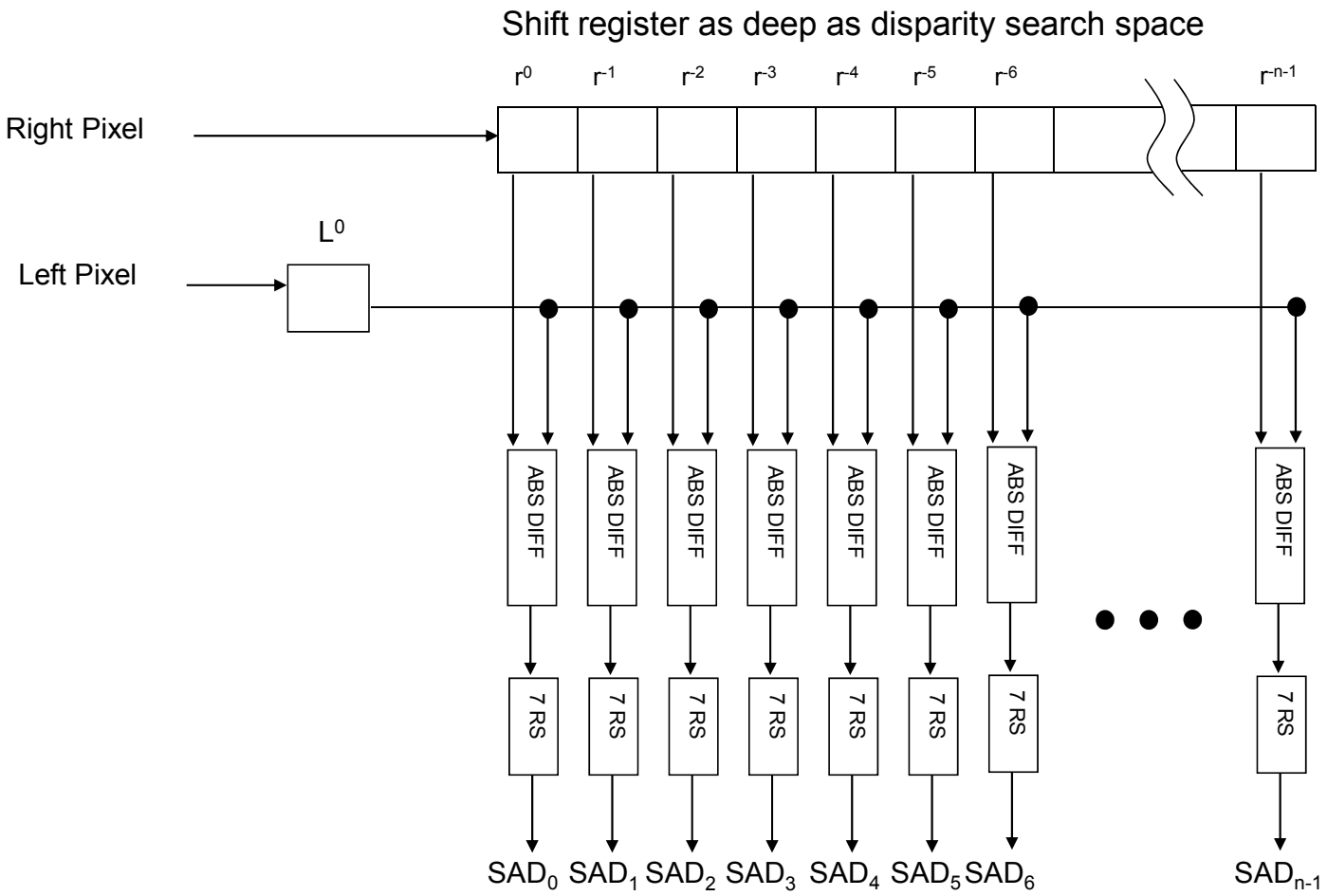
Right Image
(search image)

For a left-as-reference image, each pixel in the left image is compared against N disparity pixels in the right hand image. The search space starts at the same column as the left pixel column, and moves left. For a right-as-reference search, the search space in the left image also starts in the same column, but moves right.

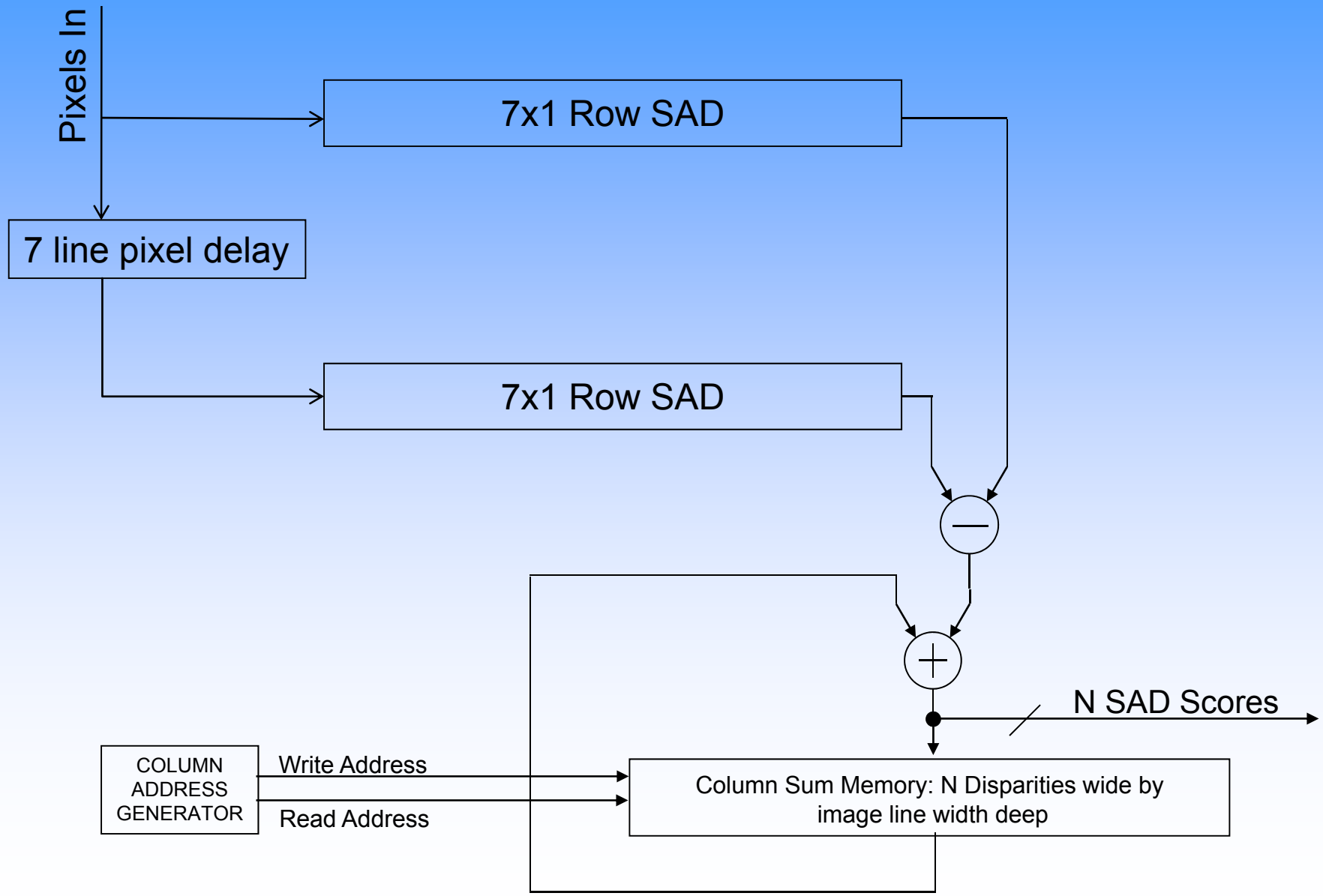
Correlation Overview



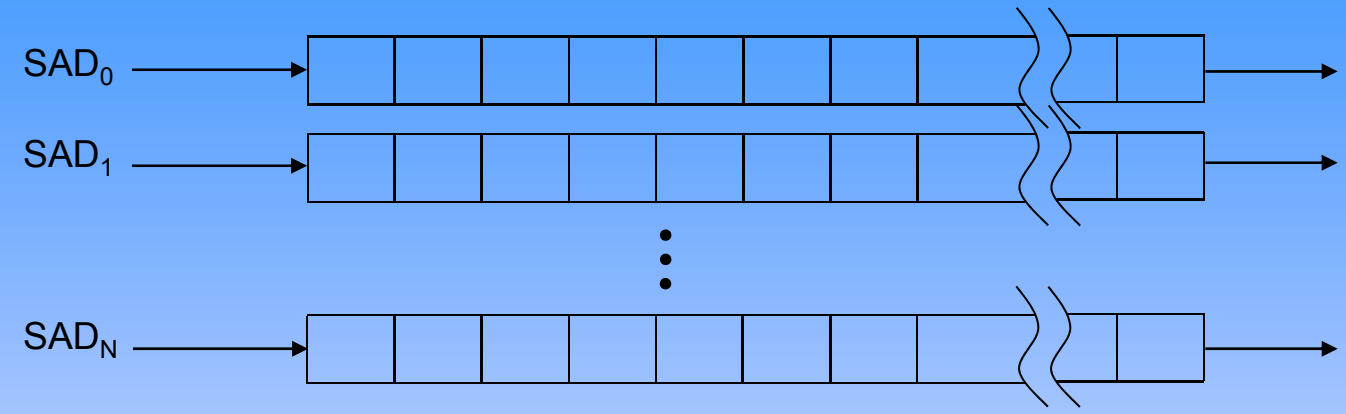
Score Generator: 7x1 subscore



Score Generator: 7x7 Score



Score Delay

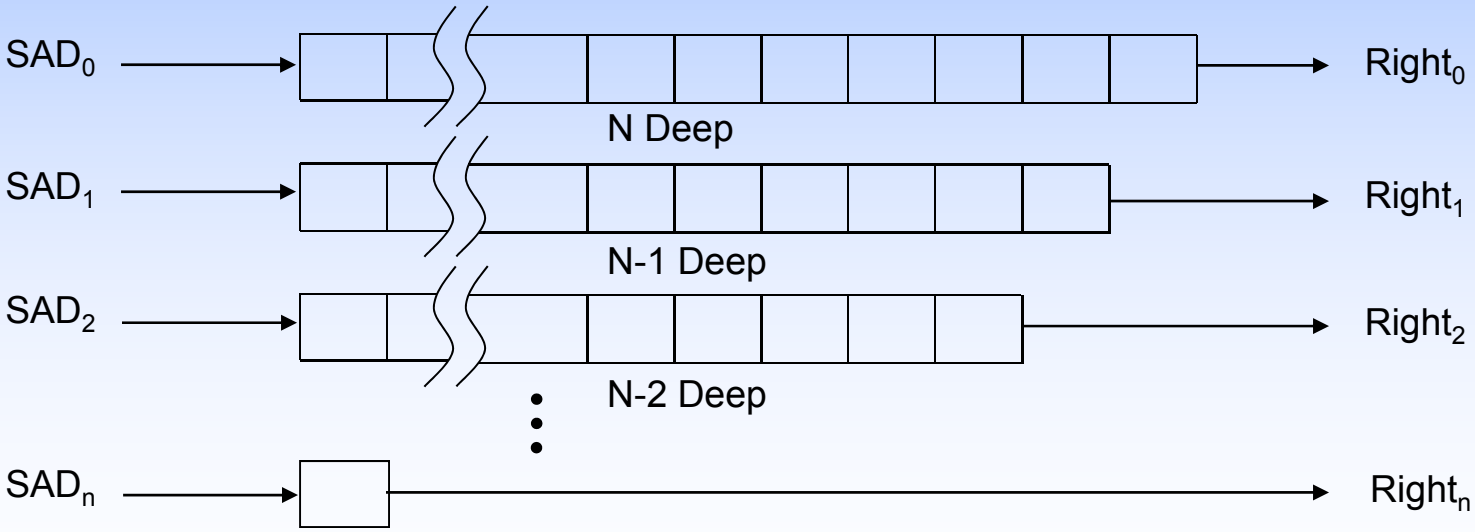


N Shift Registers: N Disparities deep

L/R Score equivalence

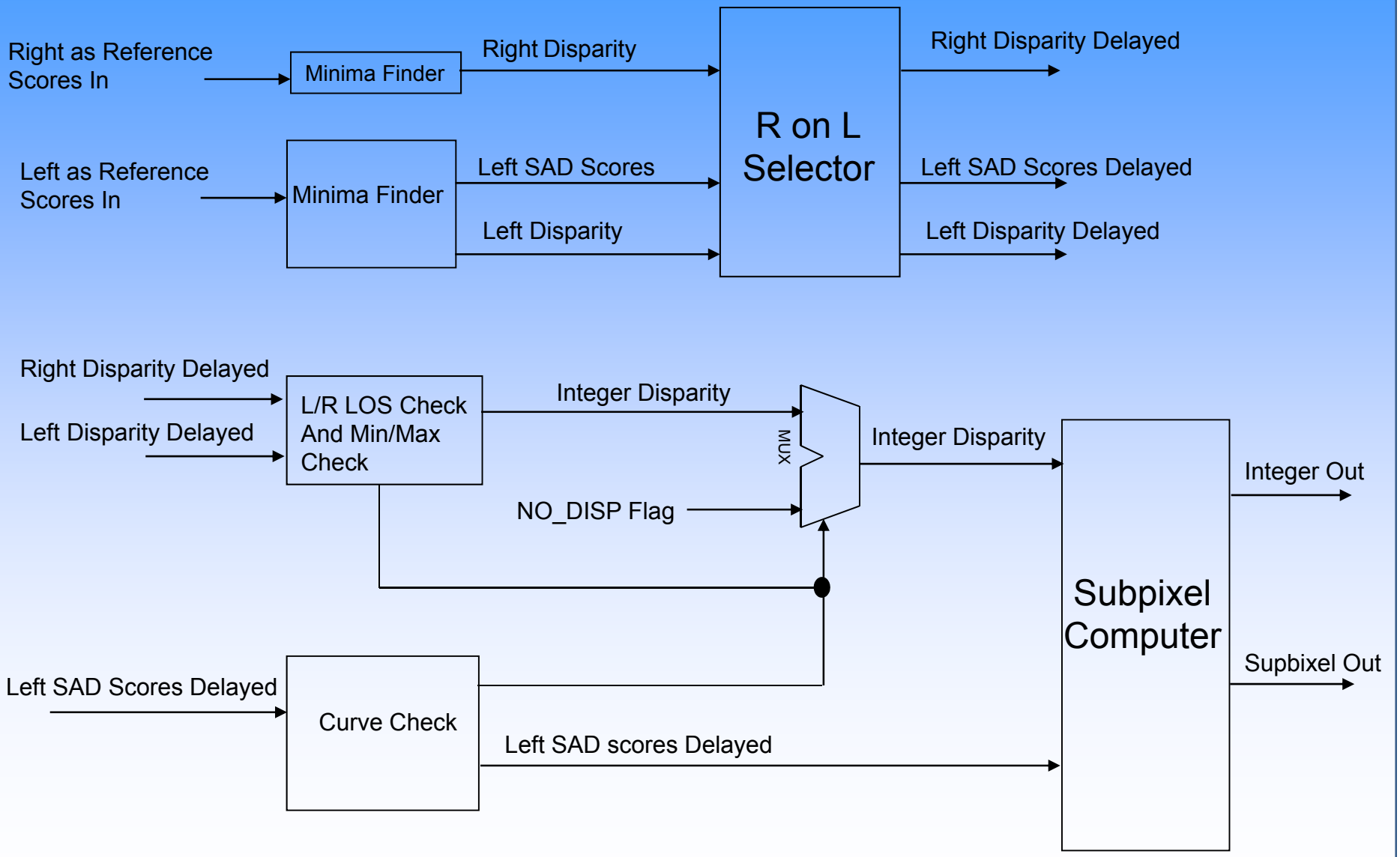
L = Left Score
R = Right Score
D = Disparity
i = Current pixel
x = Current disparity

L(i)D(x) = R(i-x)D(x)



Output of Score Delay is 2 score vectors, 1 vector with left as reference, and 1 score with right as reference

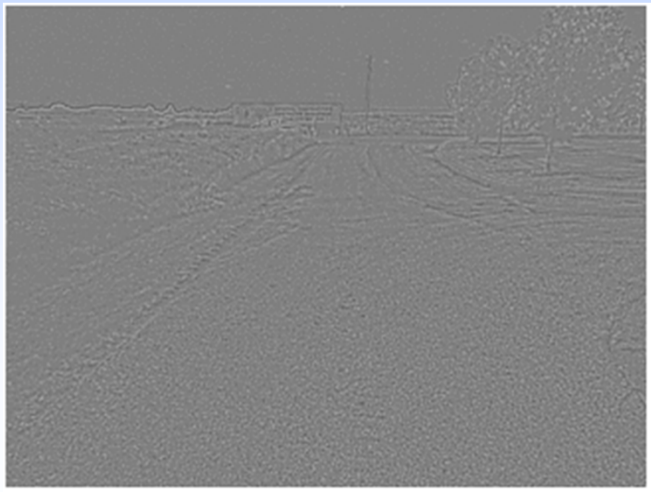
Disparity Computation



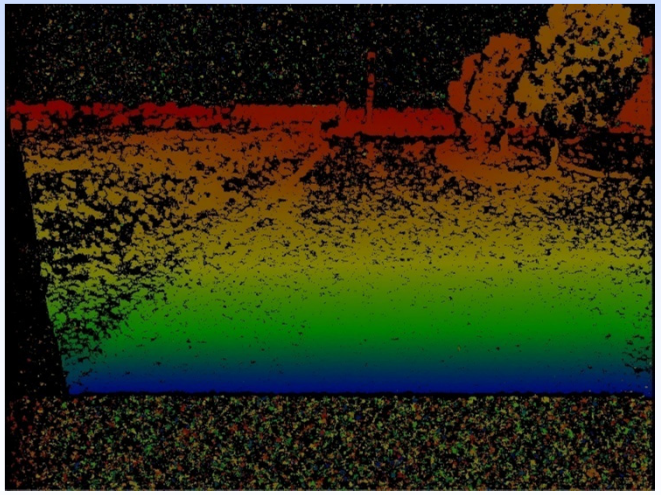
Results

Raw Image

Rectified Image



Filtered Image



Disparity Image

Results (cont.)

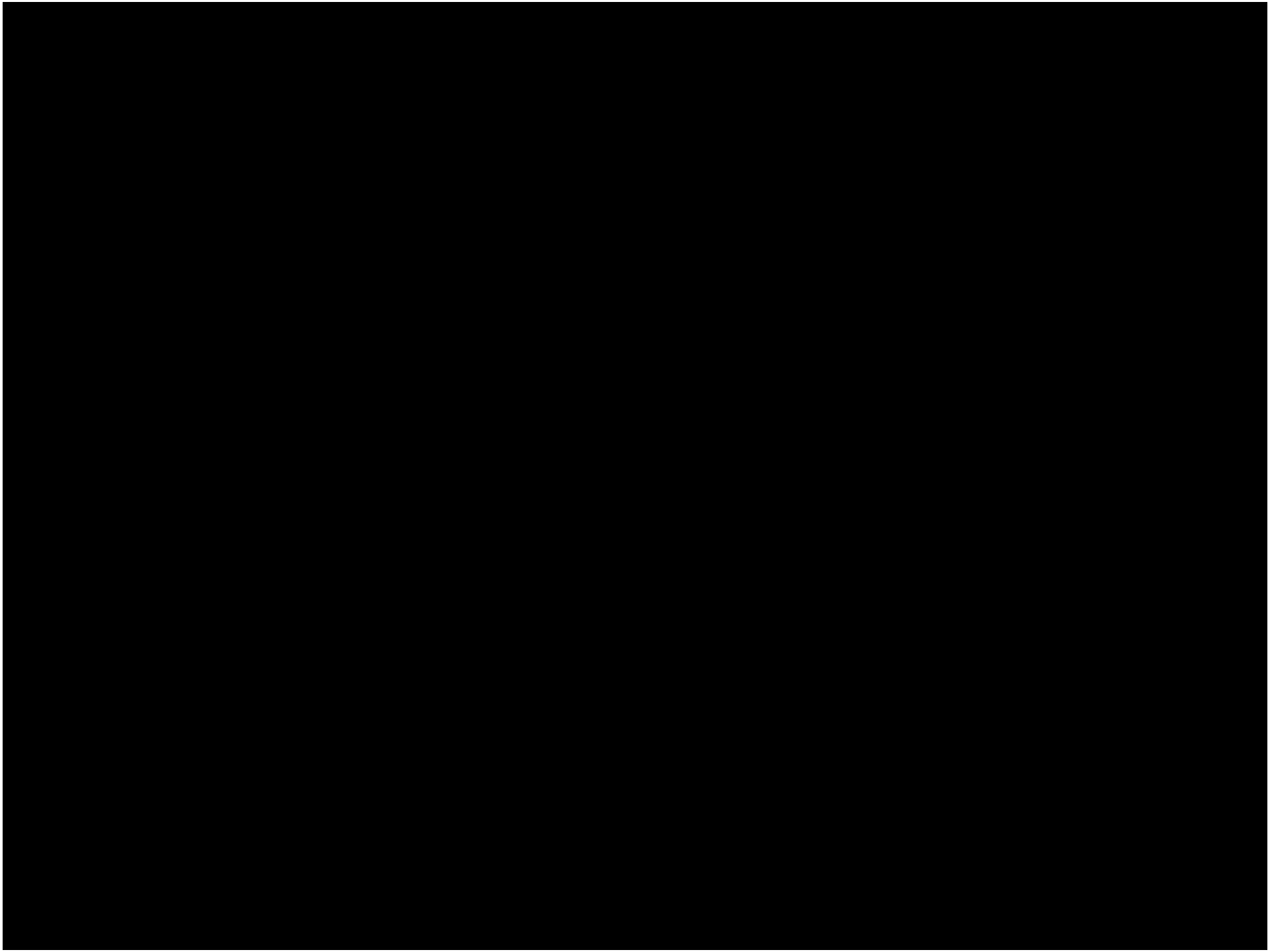
FPGA Resource usage	BRAM	Slices
Virtex 4LX160	288	67,584
Virtex 5FX130t	576	40,960
Rectification	2	1,186
Bilateral Subtraction Filter	18	19,893
Correlator@1024 wide		
SAD1:	100	28,845
SAD5:	450	35,004
Correlator@512x384		
SAD1:	36	13,275
SAD5:	128	17,502
Example Complete Systems:		
Rect + Bil + SAD1 @ 1024x768	134	49,924
Rect + Bil + SAD5 @ 512x384	162	38,581

	XEON 5160 @3GHz	Core2 QUAD @ 2.4GHz
Rectification (2 images)	3 ms	6 ms
Bilateral Subtraction Filter (2 images)	6947 ms	8734 ms
Disparity	74 ms	87 ms
Total time	7024 ms	8827 ms

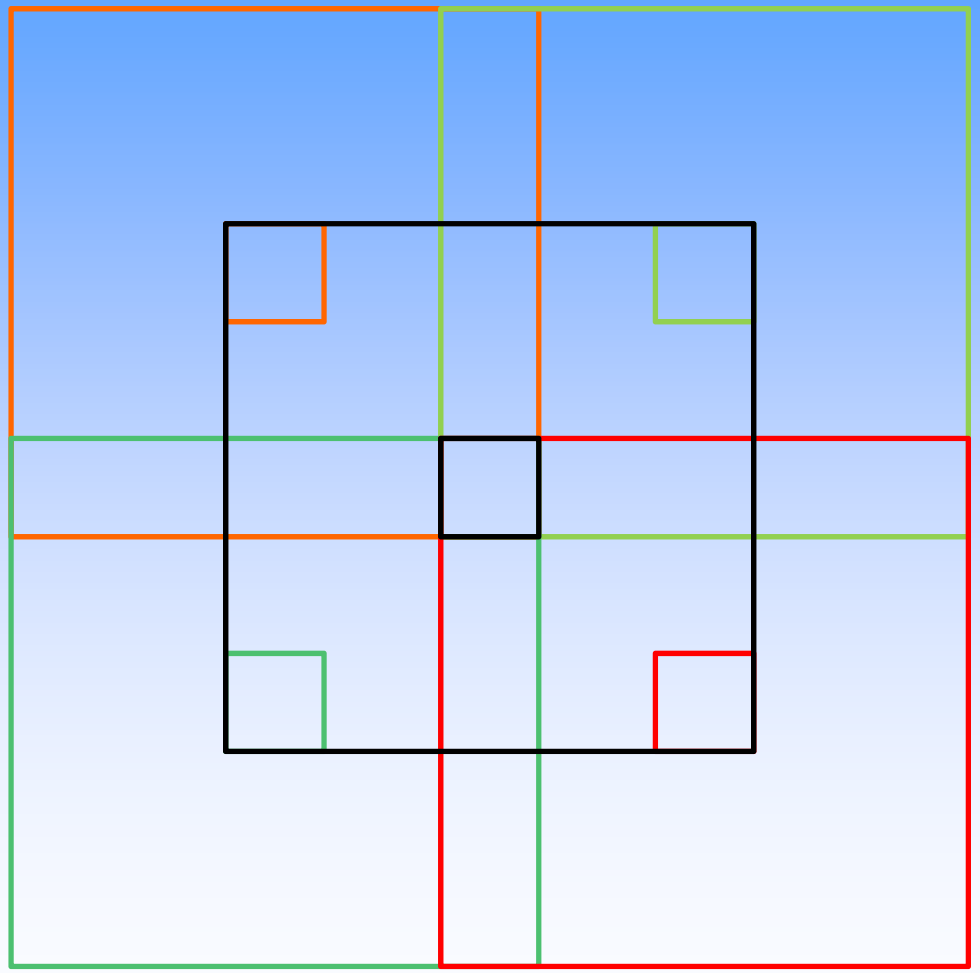
FPGA Performance @66 MHz:

Disparity with imagery: 12 Hz

Disparity only: 15 Hz



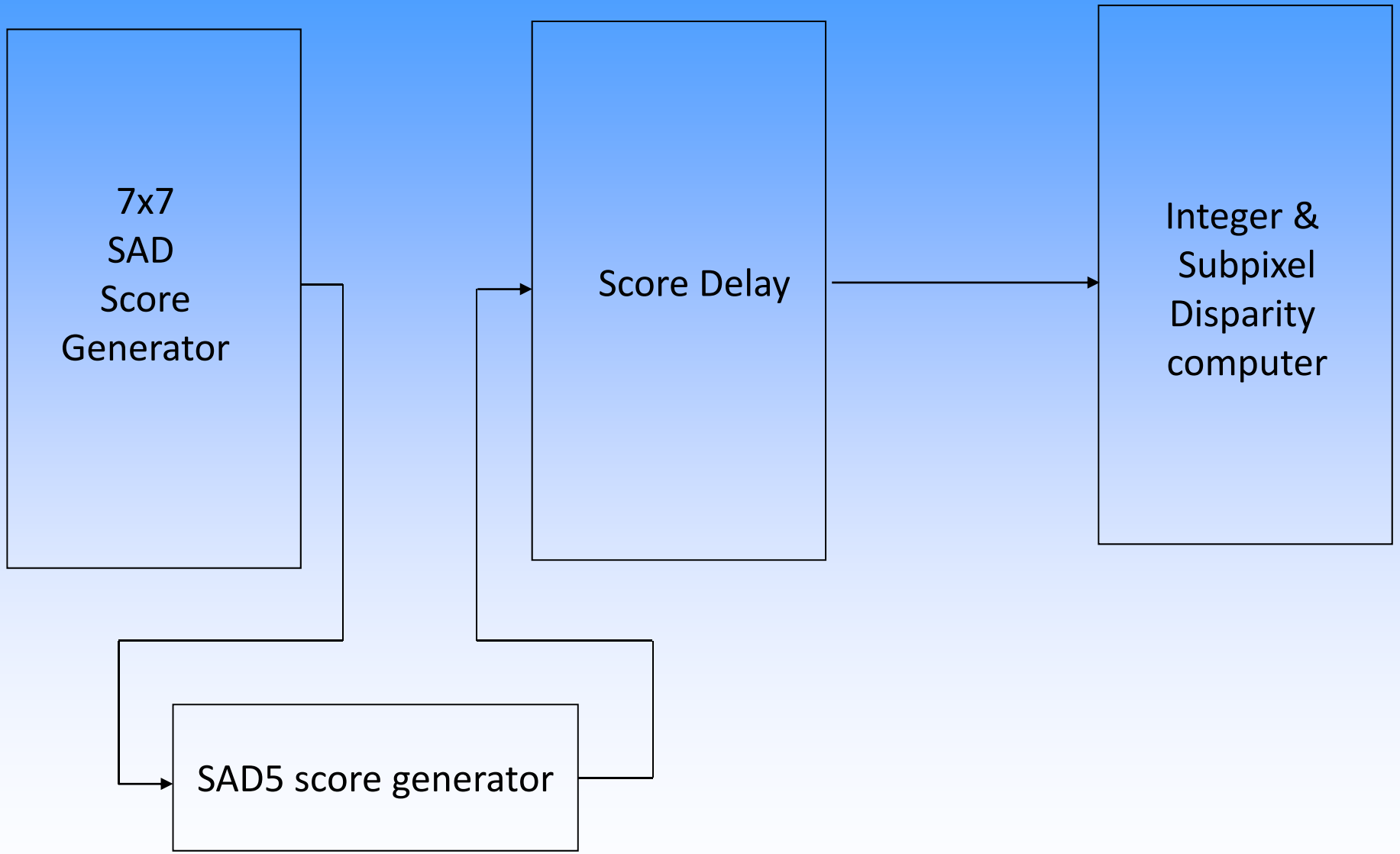
SAD5 Addition



SAD5 score vectors are a combination of the SAD1 score of the center pixel plus the lowest two SAD1 scores of the “corner” pixels at each disparity level.

Primarily used for improving range data on object edges and range discontinuities

SAD 5 Addition



SAD5 Score Generator